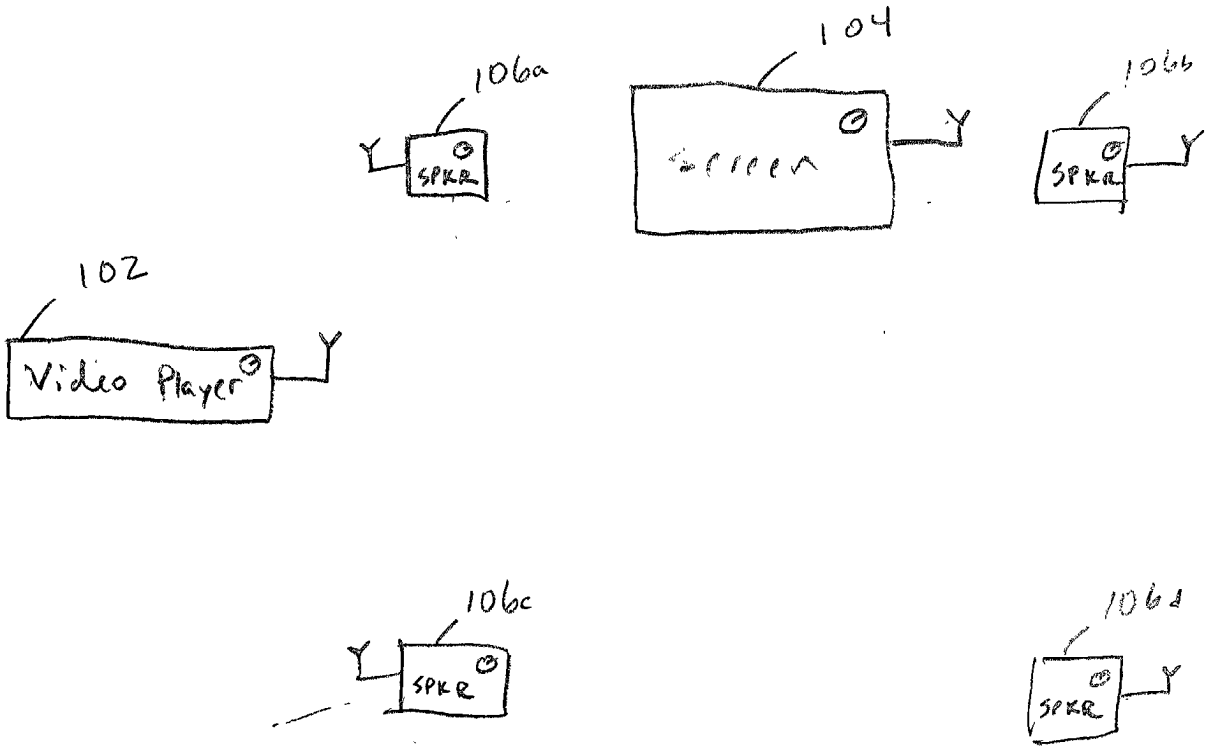


Figure 1

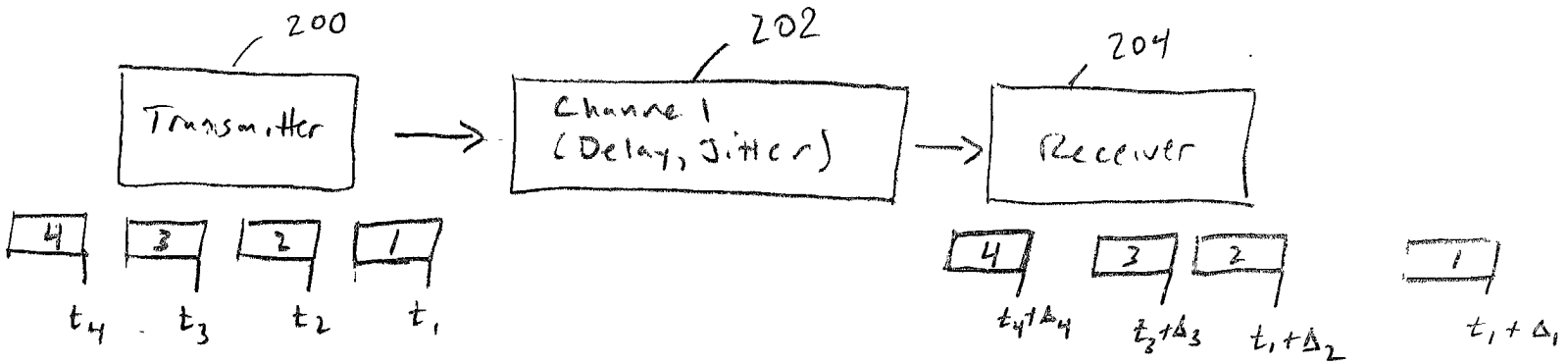


Figure 2

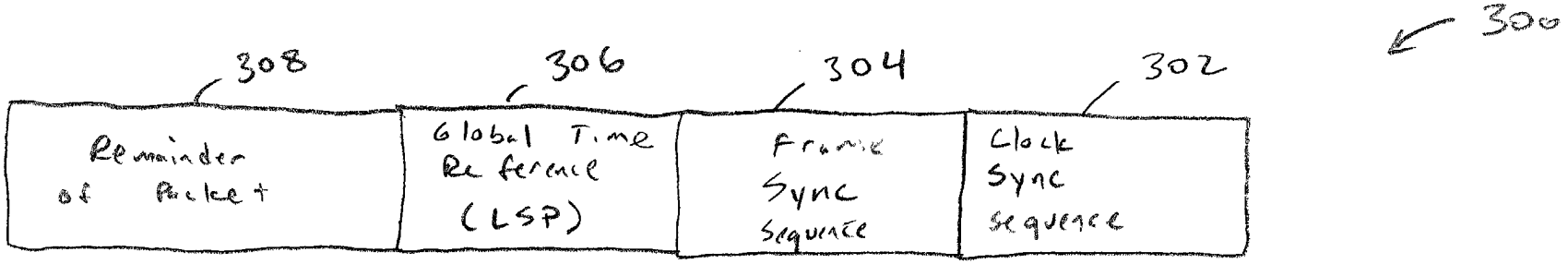


Figure 3

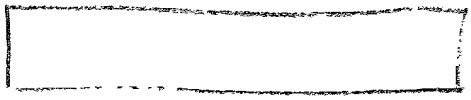
GTR

Figure 4A

20 bit 12 bit

FRC

Figure 4B



32 bit

FECO

Figure 4C

32 bit

GTR = FRC + FECO

Figure 5

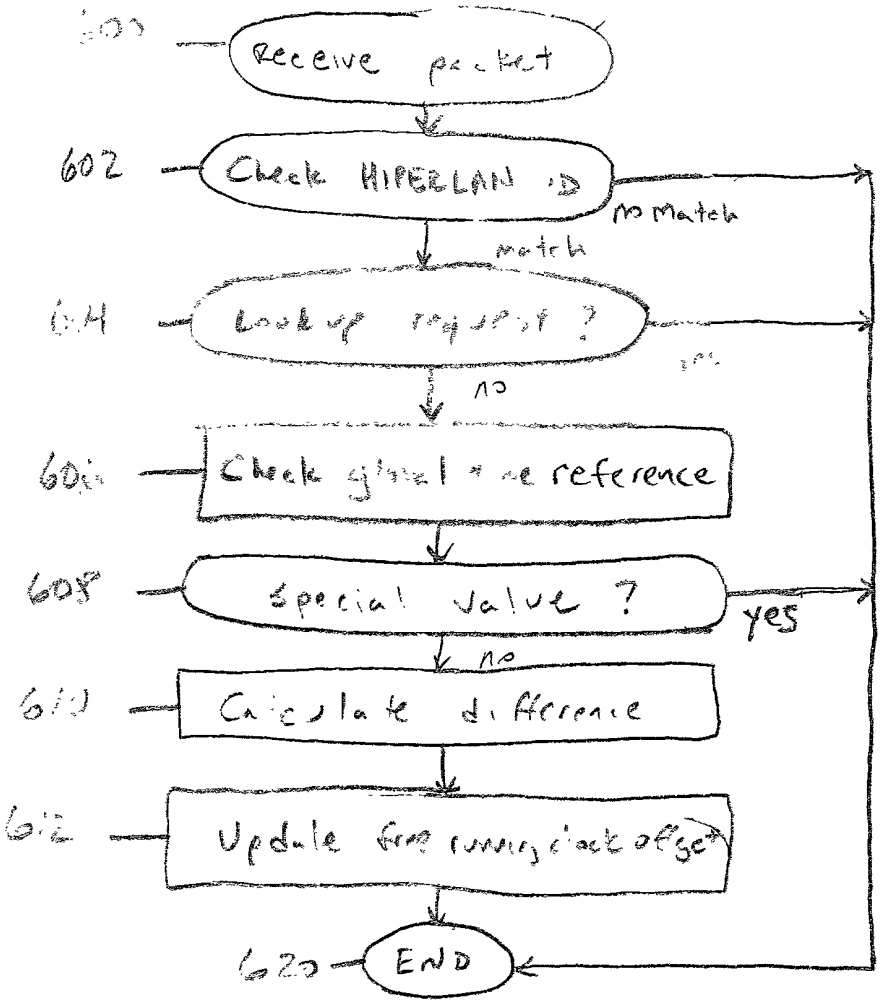

Receive packet
602
Check HIPERLAN ID
no match
match
Look up request ?
no
Check global time reference
Special value ?
yes
no
Calculate difference
Update from running clock offset
END

Figure 6

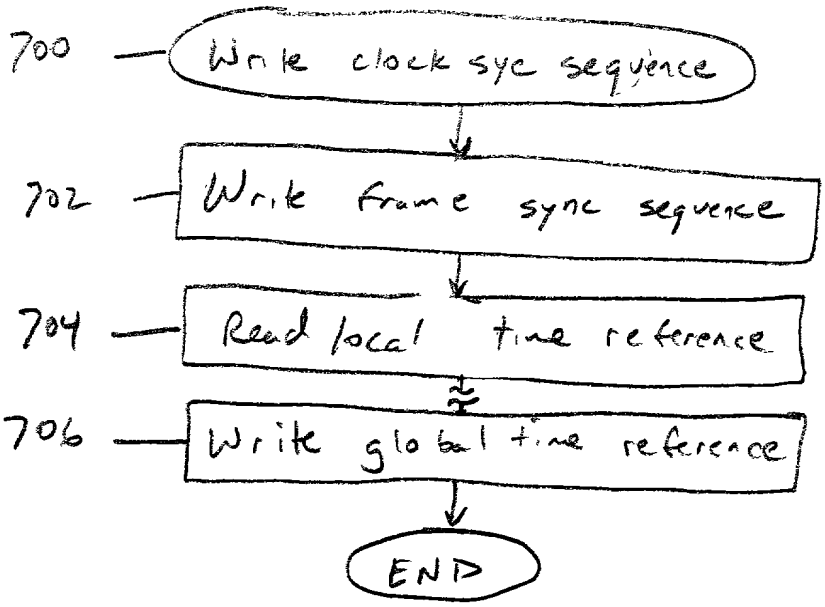


Figure 7A

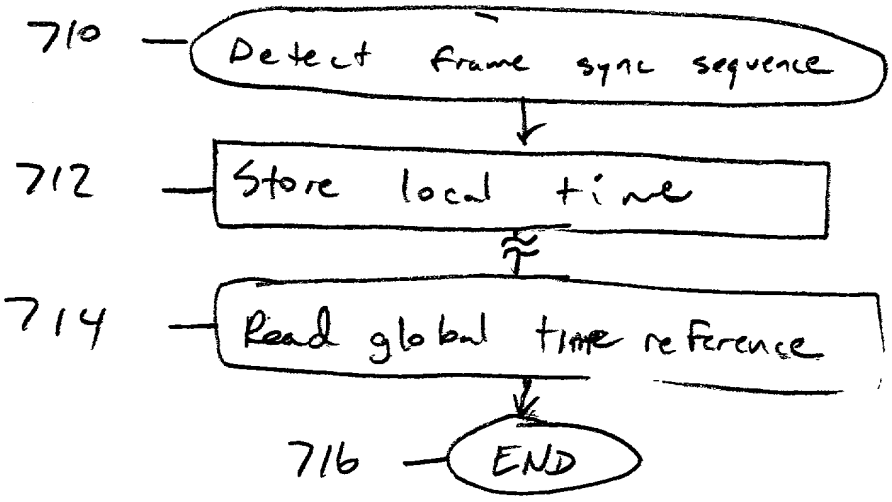


Figure 7B